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| **Cairo University** | **CMPN201** | **Total: 20 Points** |
| **Faculty of Engineering** | **Microprocessor Systems I** | **2016-2017** |
| **Computer Eng. Department** | **Midterm Exam** | **One Hour** |

**This is an open-book, open notes exam. All electronic devices - Except calculators - are forbidden.  
Make any reasonable assumptions (if necessary)  
Answer the following questions [any answer outside answer location will be discarded]**

1. [2] Increasing the external data bus width increases *data transfer speed to and from processor*
2. [4] What is the function of the following programs

|  |  |
| --- | --- |
| MOV AL,N  DEC N  LBL: MOV BL,N  MUL BL  DEC N  JNZ LBL | MOV AX,A  MOV BX,B  MUL BX |
| AX=Factorial N | AX=A\*B |

1. [4] Allocate syntax errors of the following program

|  |  |
| --- | --- |
|  | Reason |
| MOV SI, offset VAR1 | . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . |
| MOV DI, offset VAR1+10 | . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . |
| REP LOADSB | Rep should not be used with loads |
| MOV CL,[AX] | AX should not be used for this addressing mode |
| MOV BL,[2AD1H] | . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . |
| MOV AX,BL | Register size mismatch |
| MOV CL,[SI][DI]+10 | SI should not be used with DI |
| MOV CX, [BP] | . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . |

1. [4] Write a program that draws a red filled square on a white background starting at 100,100 [ Top left pixel]. Each side is 50px length. [**ANSWER ON THE BACK OF THIS PAGE**]
2. [10] Compatibility between the later and the earlier microprocessors has been a successful strategy for

the Intel family. Give two distinct examples of the modifications that demonstrate this compatibility.

Example 1: Registers extended such that all bytes, words can be addressed. (e.g. AL,AH,AX….)

Example 2: Memory modes divided into real and protected. Real mode for earlier MP

1. [2] Identify the operand addressing mode used in each of these instructions.
2. ADD DX, 15 : IMMEDIATE
3. CMP WORD PTR [BX+DI], 10 : Based indexed relative (BASE+INDEX)
4. [3] Suppose you had a different processor that was designed and operated similarly to the 8086/8088 architecture with the following differences: All of the registers are 8-bit registers, and the physical address (PA) is a 10-bit number.
5. Given what you know about the 8086/8088 architecture, what would be the size of the total addressing space on this new device?

2Address bus size =210 =1KB or 1,024 Bytes

1. Given what you know about 8086/8088 addressing, what would be the size of the “offset window” at each segment location through which you could address memory?

2IP register size = 28 = 256 **Bytes**

1. [4] What is the content of AX after executing each of the following codes?

|  |  |
| --- | --- |
| MOV AL,00000011B  MOV BL,10000000B  MUL BL | MOV AL,00000011B  MOV BL,10000000B  IMUL BL |
| 0000000110000000B=0180H= 384D | 1111111010000000 B=FE80H= -384D |

1. [2] 10101101 = 173D [as an unsigned number]

and 10101101 = -83D [as a signed number]

1. [4] Write a program that merges two sorted lists into a new list. [**ANSWER ON THE BACK OF THIS PAGE**]
2. [3] A computer manufacturer announced for a machine with 16 KB video memory and supports 320\*460 resolution. How many different colors does it support?

16\*8\*1024/ (320\*460) = 0.89 bit [2 Marks]

0.89 bit <1 (Manufacturer is liar) [1Mark]

1. [4] Write a single instruction for each of the following operations. Note that no other changes should occur.
   1. Invert bits number 0, 5, 10, and 15 in AX: XOR AX,8421H or XOR AX,1000010000100001B
   2. Divide the content of AX by 16 : SHR AX,4